We claim:

1.   A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

         initializing a first and second subset of a set of per-alignment state machines;

         receiving a first and second signal; and

         simultaneously sync hunting the first signal with the first subset of the set of per-alignment state machines and the second signal with the second subset of the set of per-alignment state machines.

2.   The machine-readable medium of claim 1 wherein the first and second signal have different formats.

3.   The machine-readable medium of claim 1 wherein the sync hunting includes updating a first and second set of states indicated by the first and second subset of the set of per-alignment state machines and writing the updated first set of states to the first subset of per-alignment state machines and the second set of states to the second subset of per-alignment state machines.

4.   The machine-readable medium of claim 1 further comprising buffering a first set of states from the first subset of the set of per-alignment state machines and a second set of states from the second subset of the set of per-alignment state machines.

5.   The machine-readable medium of claim 1 further comprising:

2   updating a first and second set of states from the first and second subset of the set of

3   per-alignment state machines;

4   buffering the first and second set of states; and

5   writing the first set of states to the first subset of the set of per-alignment state

6   machines; and

7   writing the second set of states to the second subset of the set of per-alignment state

8   machines.

1   6.   A machine-readable medium that provides instructions, which when executed by a set

2   of processors, cause said set of processors to perform operations comprising:

3   initializing a first and second subset of a set of per-alignment state machines;

4   receiving a first and second signal;

5   buffering a first and second set of states from the first and second subset of the set of

6   per-alignment state machines;

7   simultaneously sync hunting the first signal with the first set of states and the second

8   signal with the second set of states.

1   7.   The machine-readable medium of claim 6 wherein the first and second signal have

2   different formats.

1   8.   The machine-readable medium of claim 6 wherein the sync hunting includes updating

2   the first and second set of states and writing the updated first set of states to the first subset of

3   per-alignment state machines and the second set of states to the second subset of per-

4   alignment state machines.

1   9.   The machine-readable medium of claim 6 further comprising:

2   updating the first and second set of states;

3   buffering the first and second set of states;

4   writing the updated first set of states to the first subset of per-alignment state

5   machines; and

6   writing the updated second set of states to the second subset of per-alignment state

7   machines.

1   10.   A machine-readable medium that provides instructions, which when executed by a set

2   of processors, cause said set of processors to perform operations comprising:

3   initializing a first subset of a set of per-alignment state machines;

4   receiving a first signal;

5   initializing a second subset of the set of per-alignment state machines;

6   receiving a second signal;

7   buffering a first set of states from the first subset of per-alignment state machines;

8   buffering a second set of states from the second subset of per-alignment state

9   machines;

10   simultaneously sync hunting the first signal with the first set of states and the second

11   signal with the second set of states.

1   11.   The machine-readable medium of claim 10 wherein the first and second signal have

2   different formats.

1   12.   The machine-readable medium of claim 10 wherein the sync hunting includes

2   updating the first and second set of states and writing the updated first set of states to the first

3   subset of per-alignment state machines and the second set of states to the second subset of

4   per-alignment state machines.

1   13.   The machine-readable medium of claim 10 further comprising:

2   updating the first and second set of states;

3   buffering the first and second set of states;

4   writing the updated first set of states to the first subset of per-alignment state

5   machines; and

6   writing the updated second set of states to the second subset of per-alignment state

7   machines.

1   14.   An apparatus comprising:

2   a first logic to sync hunt a first signal;

3   a second logic to sync hunt a second signal;

4   a memory controller coupled to the first and second logic, the memory controller to

5   perform read and write operations; and

6   a memory unit coupled to the memory controller, the memory unit to store a set of

7   per-alignment state machines.

1   15.   The apparatus of claim 14 wherein the first and second logic are for a first and second

2   signal format.

1   16.   The apparatus of claim 14 wherein the first logic includes:

2   a read buffer coupled to the memory controller, the read buffer to buffer a first set of

3   states written by the memory controller; and

4   a write buffer coupled to the memory controller, the write buffer to buffer a second

5   set of states output from the first logic.

1   17.   The apparatus of claim 14 wherein the second logic includes:

2   a read buffer coupled to the memory controller, the read buffer to buffer a first set of

3   states written by the memory controller; and

4   a write buffer coupled to the memory controller, the write buffer to buffer a second

5   set of states output from the second logic.

1   18.   The apparatus of claim 14 further comprising:

2   a write buffer coupled to the first and second logic and the memory controller, the

3   write buffer to buffer a first set of states written by the memory controller; and

4   a read buffer coupled to the first and second logic and the memory controller, the read

5   buffer to buffer a second set of states, the second set of states written to the

6   read buffer by the first and second logic.

1   19.   The apparatus of claim 14 further comprising:

2   the first logic to update a first set of states from the memory unit;

3   the second logic to update a second set of states from the memory unit;

4   a first buffering unit coupled to the memory controller and the first logic, the first

5   buffering unit to buffer the first set of states written from the memory unit by

6   the memory controller and to buffer the updated first set of states from the

7   first logic; and

8   a second buffering unit coupled to the memory controller and the second logic, the

9   second buffering unit to buffer the second set of states written from the

10   memory unit by the memory controller and to buffer the updated second set of

11   states from the second logic.

1   20.   An apparatus comprising:

2   an memory unit to store a set of per-alignment state machines;

3   a memory controller coupled to the memory unit, the memory controller to perform

4   read and write operations to the memory unit; and

5   a plurality of logic coupled to the memory controller, the plurality of logic to perform

6   sync hunting for a plurality of signals with the set of per-alignment state

7   machines.

1 21. The apparatus of claim 20 wherein the plurality of signals have different formatting.

1 22. The apparatus of claim 20 wherein each of the plurality of logic includes:

2   a read buffer coupled to the memory controller, the read buffer to buffer a first set of

3   states written by the memory controller; and

4   a write buffer coupled to the memory controller, the write buffer to buffer a second

5   set of states to be written to the memory unit by the memory controller.

1 23. The apparatus of claim 20 further comprising:

2   a write buffer coupled to the plurality of logic and the memory controller, the write

3   buffer to buffer a first set of states written by the memory controller; and

4   a read buffer coupled to the plurality of logic and the memory controller, the read

5   buffer to buffer a second set of states, the second set of states written to the

6   read buffer by the plurality of logic.

1 24. The apparatus of claim 20 further comprising:

2   the plurality of logic to update a set of states from the memory unit; and

3   a buffering unit coupled to the memory controller and the plurality of logic, the

4   buffering unit to buffer the set of states written from the memory unit by the

5   memory controller and to buffer the updated set of states from the plurality of

6   logic.

1 25. An apparatus comprising:

2   a memory unit to store a set of per-alignment state machines;

3   a memory controller coupled to the memory unit to access the set of per-alignment

4   state machines;

5   a first deframing slice coupled to the memory controller, the first deframing slice to

6   sync hunt a first signal with a first subset of the set of per-alignment state

7   machines; and

8   a second deframing slice coupled to the memory controller, the second deframing

9   slice to sync hunt a second signal with a second subset of the set of per-

10   alignment state machines.

1 26. The apparatus of claim 25 wherein the first and second signal have different signal

2 formatting.

1 27. The apparatus of claim 25 wherein the first deframing slice includes a first logic for a

2 first signal format and a second logic for a second signal format.

1 28. The apparatus of claim 25 wherein the first deframing slice includes:

2   a read buffer coupled to the memory controller, the read buffer to buffer a first set of

3   states from the first subset of per-alignment state machines written by the

4   memory controller; and

5   a write buffer coupled to the memory controller, the write buffer to buffer a second

6   set of states output from the first deframing slice.

1 29. The apparatus of claim 25 wherein the second deframing slice includes:

2   a read buffer coupled to the memory controller, the read buffer to buffer a first set of

3   states from the second subset of per-alignment state machines written by the

4   memory controller; and

5   a write buffer coupled to the memory controller, the write buffer to buffer a second

6   set of states output from the second deframing slice.

1 30. The apparatus of claim 25 further comprising:

2   a write buffer coupled to the first and second deframing slice and the memory

3   controller, the write buffer to buffer a first set of states written by the memory

4   controller; and

5   a read buffer coupled to the first and second deframing slice and the memory

6   controller, the read buffer to buffer a second set of states, the second set of

7   states written to the read buffer by the first and second deframing slice.

1 31. The apparatus of claim 25 further comprising:

2   the first deframing slice to update a first set of states from the memory unit;

3   the second deframing slice to update a second set of states from the memory unit;

4   a first buffering unit coupled to the memory controller and the first deframing slice,

5   the first buffering unit to buffer the first set of states written from the memory

6   unit by the memory controller and to buffer the updated first set of states from

7   the first deframing slice; and

8   a second buffering unit coupled to the memory controller and the second deframing

9   slice, the second buffering unit to buffer the second set of states written from

10   the memory unit by the memory controller and to buffer the updated second

11   set of states from the second deframing slice.

1   32.   An apparatus comprising:

2   a memory unit to store a set of per-alignment state machines;

3   a memory controller coupled to the memory unit, the memory controller to access the

4   set of per-alignment state machines;

5   a first deframing slice coupled to the memory controller, the first deframing slice

6   having

7   a first set of buffers coupled to the memory controller, the first set of buffers

8   to store a first set of states from a first subset of the set of per-

9   alignment state machines,

10   a first set of logic coupled to the first set of buffers, the first set of logic to

11   sync hunt a first signal with the first set of states and to update the first

12   set of states,

13   a second set of buffers coupled to the first set of logic, the second set of

14   buffers to store the updated first set of states, the updated first set of

15   states to be written to the first subset of the set of per-alignment state

16   machines; and

17   a second deframing slice coupled to the memory controller, the second deframing

18   slice having

19   a third set of buffers coupled to the memory controller, the third set of buffers

20   to store a second set of states from a second subset of the set of per-

21   alignment state machines,

22   a second set of logic coupled to the third set of buffers, the second set of logic

23   to sync hunt a second signal with the second set of states and to update

24   the second set of states,

25   a fourth set of buffers coupled to the second set of logic, the fourth set of

26   buffers to store the updated second set of states, the updated second set

27   of states to be written to the second subset of the set of per-alignment

28   state machines.

1   33.   The apparatus of claim 32 wherein the first and second signal have different signal

2   formatting.

1   34.   The apparatus of claim 32 wherein the first deframing slice further comprises a third

2   set of logic for a second signal format, the first set of logic being for a first signal format.

1   35.   A computer implemented method comprising:

2   initializing a first and second subset of a set of per-alignment state machines;

3   receiving a first and second signal; and

4   simultaneously sync hunting the first signal with the first subset of the set of per-

5   alignment state machines and the second signal with the second subset of the

6   set of per-alignment state machines.

1   36.   The computer implemented method of claim 35 wherein the first and second signal

2   have different formats.

1   37.   The computer implemented method of claim 35 wherein the sync hunting includes

2   updating a first and second set of states indicated by the first and second subset of the set of

3   per-alignment state machines and writing the updated first set of states to the first subset of

4   per-alignment state machines and the second set of states to the second subset of per-

5   alignment state machines.

1   38.   The computer implemented method of claim 35 further comprising buffering a first

2   set of states from the first subset of the set of per-alignment state machines and a second set

3   of states from the second subset of the set of per-alignment state machines.

1   39.   The computer implemented method of claim 35 further comprising:

2   updating a first and second set of states from the first and second subset of the set of

3   per-alignment state machines;

4   buffering the first and second set of states; and

5   writing the first set of states to the first subset of the set of per-alignment state

6   machines; and

7   writing the second set of states to the second subset of the set of per-alignment state

8   machines.

1   40.   A computer implemented method comprising:

2   initializing a first and second subset of a set of per-alignment state machines;

3   receiving a first and second signal;

4   buffering a first and second set of states from the first and second subset of the set of

5   per-alignment state machines;

6   simultaneously sync hunting the first signal with the first set of states and the second

7   signal with the second set of states.

1   41.   The computer implemented method of claim 40 wherein the first and second signal

2   have different formats.

1   42.   The computer implemented method of claim 40 wherein the sync hunting includes

2   updating the first and second set of states and writing the updated first set of states to the first

3   subset of per-alignment state machines and the second set of states to the second subset of

4   per-alignment state machines.

1   43.   The computer implemented method of claim 40 further comprising:

2   updating the first and second set of states;

3   buffering the first and second set of states;

4   writing the updated first set of states to the first subset of per-alignment state

5   machines; and

6   writing the updated second set of states to the second subset of per-alignment state

7   machines.

1   44.   A computer implemented method comprising:

2   initializing a first subset of a set of per-alignment state machines;

3   receiving a first signal;

4   initializing a second subset of the set of per-alignment state machines;

5   receiving a second signal;

6   buffering a first set of states from the first subset of per-alignment state machines;

7   buffering a second set of states from the second subset of per-alignment state

8   machines;

9   simultaneously sync hunting the first signal with the first set of states and the second

10   signal with the second set of states.

1   45.   The computer implemented method of claim 44 wherein the first and second signal

2   have different formats.

1   46.   The computer implemented method of claim 44 wherein the sync hunting includes

2   updating the first and second set of states and writing the updated first set of states to the first

3   subset of per-alignment state machines and the second set of states to the second subset of

4   per-alignment state machines.

1   47.   The computer implemented method of claim 44 further comprising:

2   updating the first and second set of states;

3   buffering the first and second set of states;

4   writing the updated first set of states to the first subset of per-alignment state

5   machines; and

6   writing the updated second set of states to the second subset of per-alignment

7   state machines.